



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,882	09/09/2003	Kuo-Tung Chang	AMD-H0642	3204
7590 10/12/2005			EXAMINER	
WAGNER, MURABITO & HAO LLP			LEE, EUGENE	
Third Floor			ART UNIT	
Two North Market Street			PAPER NUMBER	
San Jose, CA 95113			2815	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

28

Office Action Summary	Application No. 10/658,882	Applicant(s) CHANG ET AL.	
	Examiner Eugene Lee	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 September 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/7/05 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 8, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Karp et al. 6,266,269 B1. Karp discloses (see, for example, FIG. 2C) a programmed storage transistor (integrated circuit device) 205 comprising diffusions (lateral diffusions of source and drain implantation regions) 206 that overlap.

Regarding the limitation “parameters comprising dopant species, dopant concentration, implant energy, temperature, and duration are controlled during manufacture such that said manufacture achieves...” in claim 8, this limitation is a product-by-process limitation that does not add any new structural limitations to the applicant’s claimed product (i.e. “first region under

a gate that comprises overlapping lateral diffusions of source and drain implantation regions”).

Therefore, Karp still discloses the applicant’s claimed product.

Regarding claim 14, see the abstract wherein Karp discloses a non-volatile memory element.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1 thru 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrad et al. 6,765,257 B1 in view of Karp et al. 6,266,269 B1. Mehrad discloses (see, for example, FIG. 1) a memory (integrated circuit device) comprising an array of memory elements (cells), said memory elements comprising a source, a drain and a gate; horizontal source line (common source line) 17, and source contact 32. Mehrad does not disclose a region under said gate manufactured such that said region comprises overlapping lateral diffusions of implantation regions of said source and said drain. However, Karp discloses (see, for example, FIG. 2C) a programmed storage transistor (integrated circuit device) 205 comprising diffusions (lateral diffusions of source and drain implantation regions) 206 that overlap. In column 7, lines 13-42, Karp discloses that the single diffusion region provides a permanent conductive path, which enhances reliability and decreases feature size. Therefore, it would have been obvious to one of

Art Unit: 2815

ordinary skill in the art at the time of invention to have a region under said gate manufactured such that said region comprises overlapping lateral diffusions of implantation regions of said source and said drain in order to enhance reliability and decrease feature size.

Regarding claim 2, see, for example, FIG. 1, wherein Mehrad discloses the control gate line (substantially straight word lines) 15.

Regarding claim 3, see, for example, FIG. 1, wherein Mehrad discloses the horizontal source line 17 having a substantially uniform width.

Regarding claim 4, see, for example, FIG. 1, wherein Mehrad discloses a drain contact 34 in the same row as source contact 32.

Regarding claim 5, see, for example, FIG. 2, wherein Mehrad discloses the source contact 32 coupled to the horizontal source line 17 under a gate (gate structure) 13.

Regarding claim 6, see, for example, column 1, lines 12-13, wherein Mehrad discloses a FLASH memory array which is non-volatile memory.

Regarding claim 7, see, for example, FIG. 1 wherein Mehrad discloses a floating gate 13.

6. Claims 9 thru 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al. '269 B1 as applied to claims 8, and 14 above, and further in view of Mehrad et al. 6,765,257 B1. Karp does not disclose one of said implantation regions being coupled to a first source contact. However, Mehrad discloses (see, for example, FIG. 2) a memory comprising a source diffusion (one of said implantation regions) and a source contact (first source contact) 32. It would have been obvious to one of ordinary skill in the art at the time of invention to have one of

Art Unit: 2815

said implantation regions being coupled to a first source contact in order to have a medium to apply a voltage to the diffusions for the operation of the transistor.

Regarding claims 10 and 13, Karp does not disclose one of said implantation region being coupled to a common source line. However, Mehrad discloses (see, for example, FIG. 2) a horizontal source line 17, which couples source diffusions. The horizontal source line makes it possible to make one source region that is shared between multiple cells. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have one of said implantation region being coupled to a common source line in order to form a one source region that can be shared between multiple cells in a memory array.

Regarding claim 11 and the limitation “further comprising a second gate”, see, for example, FIG. 2 wherein Mehrad discloses multiple gates (gate and second gate) 13. Regarding the limitation “parameters comprising dopant species, dopant concentration, implant energy, temperature, and duration are controlled during manufacture such that said manufacture achieves...”, this limitation is a product-by-process limitation that does not add any new structural limitations to the applicant’s claimed product (i.e. “second region under said second gate comprises overlapping lateral diffusions of source and drain implantation regions”). Therefore, Karp in view of Mehrad still discloses the applicant’s claimed product.

Regarding claim 12, see, for example, FIG. 2 wherein Mehrad discloses multiple source contacts (first source contact, and second source contact) 32.

Response to Arguments

7. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
October 5, 2005

